GATE QUESTIONS

A.Y.: 2021-2022 (Odd SEM) **Scheme: CBCGS-HME 2020**

Class: S.E. E&TC Subject: Digital Logic Design

1 mark sample questions

1. Which of the following is an invalid state in 8-4-2-1 Binary Coded Decimal counter?

   a. 1000
   b. 1001
   c. 0011
   d. 1100

2. The Boolean expression $AB + A\overline{C} + BC$ simplifies to

   a. $BC + A\overline{C}$
   b. $AB + A\overline{C} + B$
   c. $AB + A\overline{C}$
   d. $AB + BC$

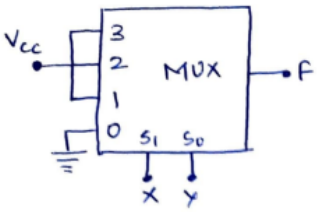
3. What is the equivalent 2's complement representation of a 2's complement no. 1001?

   a. 001001
   b. 011001
   c. 101001
   d. 111001

4. Circuit for comparing 2 n-bit numbers has ____ entries in truth table.

   a. 2^n
   b. n
   c. 2^{2n}
   d. 2n

5. The output F of the 4-to-1 MUX shown in figure is



a. $\overline{XY} + X$
b. $X + Y$
c. $\bar{X} + \bar{Y}$
d. $X\bar{Y} + Y$

6. Digital input signals A, B, C with A as the MSB and C as the LSB are used to realize the Boolean function F = $m_0 + m_2 + m_3 + m_5 + m_7$, where m_i denotes the i^{th} minterm. In addition, F has a don't care for m_1. The simplified expression for F is given by:

a. $\bar{A}\bar{C} + \bar{B}C + AC$
b. $\bar{A} + C$
c. $\bar{C} + A$
d. $\bar{A}C + BC + A\bar{C}$

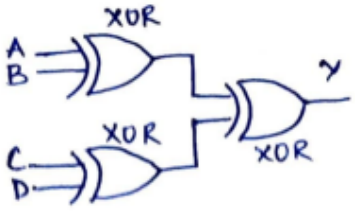
7. A cascade of three identical modulo-5 counters has an overall modulus of

a. 5
b. 25
c. 125
d. 625

8. Race condition always arises in a ____?

a. Digital circuit
b. Synchronous circuit
c. Asynchronous circuit
d. Combination circuit

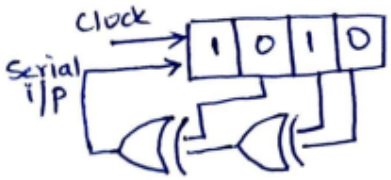
9. A, B, C, and D are input bits, and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct?



a. S is always either zero or odd
b. S is always either zero or even

c. S = 1 only if the sum of A, B, C, and D is even
d. S = 1 only if the sum of A, B, C, and D is odd

10. The shift register shown in figure. Is initially loaded with the bit pattern 1010. Sequential acts. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?

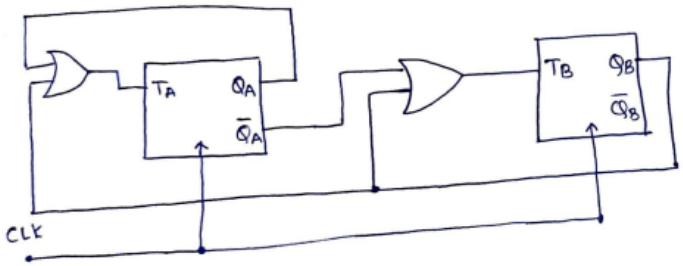


a. 3
b. 7
c. 11
d. 15

11. f(A,B,C,D) = Π M (0,1,3,4,5,7,9,11,12,13,14,15) is a max-term representation of a Boolean function f(A,B,C,D) where A is the MSB and D is the LSB. The equivalent minimized representation of this function is ____.

a. $(A + \bar{C} + D)(\bar{A} + B + D)$
b. $A\bar{C}D + \bar{A}BD + \bar{A}BC$
c. $\bar{A}C\bar{D} + A\bar{B}C\bar{D} + A\bar{B}\bar{C}\bar{D}$
d. $(B + \bar{C} + D)(A + \bar{B} + \bar{C} + D)(\bar{A} + B + C + D)$

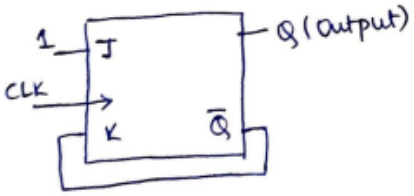
12. In the circuit shown above which transition is not possible – (Q_A Q_B → Q_A Q_B)



a. 01 → 10
b. 01 → 11
c. 11 → 00
d. 00 → 01

13. Minimum number of 3-input NAND gates required to implement the function F = $\bar{A}BD + \bar{A}CD + A\bar{B}\bar{C} + ABC\bar{D}$ is---------- (Assume Complemented variables are available)

14. Initial state: Q = 0. The output sequence Q of the circuit shown above is–



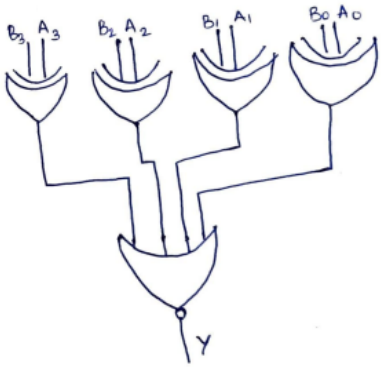
a. 0000 …….
b. 1010101 ……..
c. 11111 …….
d. 11001100 …….

15. A J. K flip flop can be made from an S.R flip –flop by using two additional
a. AND gates
b. OR gates
c. NOT gates
d. NOR gates

16. Which of the following function reflects odd parity generator?
a. $(A \oplus B) \oplus C$
b. $(A \odot B) \odot C$
c. $A \oplus (B \odot C)$
d. None of The Above

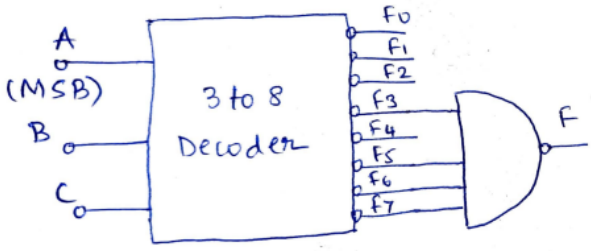
17. Which of the following counter results in least delay?
a. Asynchronous counter
b. Ripple counter
c. Synchronous counter
d. All the above

18. A digital circuit which compares two numbers $A_3A_2A_1A_0$, $B_3B_2B_1B_0$ is shown in figure. To get output Y = 0, choose one pair of correct input numbers



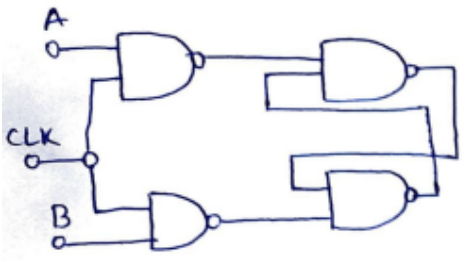
a. 1010, 1010
b. 0101, 0101
c. 0010, 0010
d. 0010, 1011

19. The function F realized by the below circuit is:



a. A+B+C
b. A′B′C′
c. AB+BC+CA
d. Π(3,5,6,7)

20. Consider the given circuit. In this circuit, the race around



a. Does not occur
b. Occurs when CLK = 0
c. Occurs when CLK = 1 and A = B = 1
d. Occurs when CLK = 1 and A = B = 0

2 mark sample questions

1. If a mod – 6 counter is constructed using 3 flip flops, the counter will skip how many counts? _____

2. A sequence detector is designed to detect precisely 3 digital inputs, with overlapping sequences detectable. For the sequence (1,0,1) and input data (1,1,0,1,0,0,1,1,0,1,0,1,1,0), what is the output of this detector?

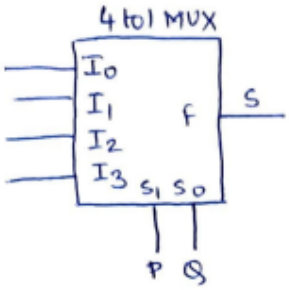
a. 1,1,0,0,0,0,1,1,0,1,0,0
b. 0,1,0,0,0,0,0,1,0,1,0,0
c. 0,1,0,0,0,0,0,1,0,1,1,0
d. 0,1,0,0,0,0,0,0,1,0,0,0

3. In the sum of products function (X,Y,Z)=∑(2,3,4,5)(X,Y,Z)=∑ (2,3,4,5), the prime implicants are

a. $\bar{X}Y, X\bar{Y}$
b. $\bar{X}Y, X\bar{Y}\bar{Z}, X\bar{Y}Z$
c. $\bar{X}Y\bar{Z}, \bar{X}YZ, X\bar{Y}$
d. $\bar{X}Y\bar{Z}, \bar{X}YZ, X\bar{Y}\bar{Z}, X\bar{Y}Z$

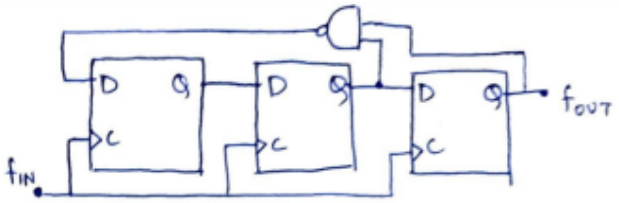
4. A 4 bit module 16 ripple counter uses JK flip-flop. If the propagation delay of each flip flop is 100 ns, the maximum clock frequency that can be used is _____(in MHz).

5. The figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in}. Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S?



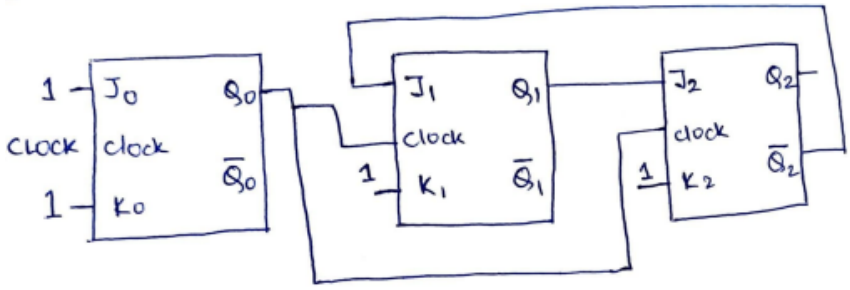
a. $I_0 = I_1 = C_{in}; I_2 = I_3 = \overline{C_{in}}$
b. $I_0 = I_1 = \overline{C_{in}}; I_2 = I_3 = C_{in}$
c. $I_0 = I_3 = C_{in}; I_1 = I_2 = \overline{C_{in}}$
d. $I_0 = I_3 = \overline{C_{in}}; I_1 = I_2 = C_{in}$

6. Which one of the following statements is true about the digital circuit shown in the figure?

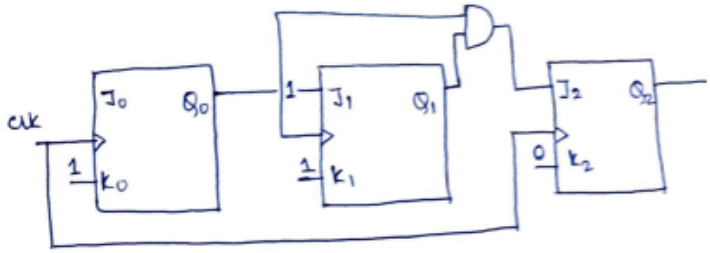


a. It can be used for dividing the input frequency by 3.
b. It can be used for dividing the input frequency by 5.
c. It can be used for dividing the input frequency by 7.
d. It cannot be reliably used as a frequency divider due to disjoint internal cycles.

7. The figure shows a digital circuit constructed using the negative edge triggered J-K flip-flops. Assume a starting state of $Q_2Q_1Q_0 = 000$. This state will repeat after how many cycles of the CLK? _____



8. In the following digital circuit the worst case delay of FFs is 40 nsec and the AND gate has delay of 20 nsec. The maximum clock frequency of the circuit to operate is ____



a. 10 MHz
b. 100 / 7 MHz
c. 50/7 MHz
d. 1 MHz

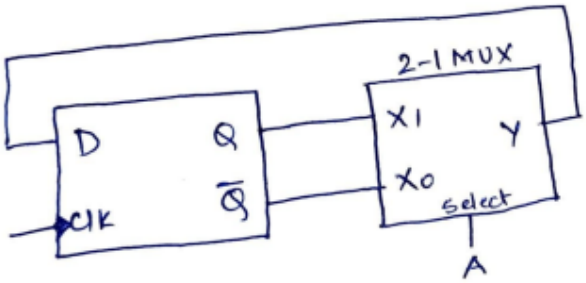
9. An X-Y flip-flop whose characteristic table is given below is to be implemented using a J-K flip-flop

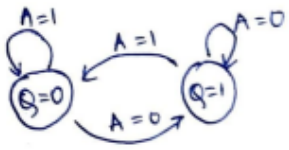
X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\bar{Q}_n$
1	1	0

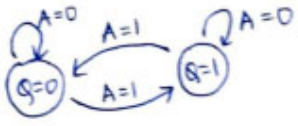
This can be done using-

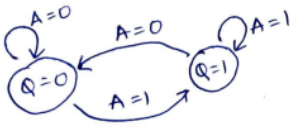
a. J = X, K = $\bar{Y}$
b. J = Y, K = $\bar{X}$
c. J = $\bar{X}$, K = Y
d. J = $\bar{Y}$, K = X

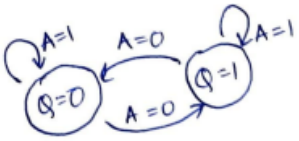
10. The state transition diagram for the logic circuit shown is



a.


b.


c.


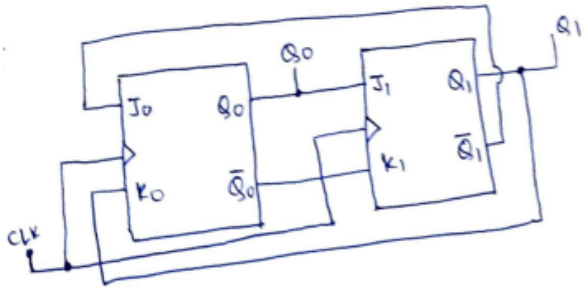
d.


11. The SOP (sum of products) form of a Boolean function is $\sum(0,1,3,7,11)$, where inputs are A, B, C, D (A is MSB, and D is LSB). The equivalent minimized expression of the function is:

a. $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{B})(\bar{C}+D)$
b. $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(\bar{C}+D)$
c. $(\bar{B}+C)(\bar{A}+C)(\bar{A}+\bar{C})(C+D)$
d. $(\bar{B}+C)(A+\bar{B})(\bar{A}+\bar{B})(\bar{C}+D)$

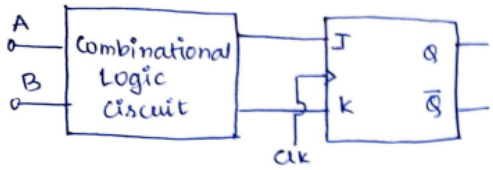
12. Statement I: We require the same no. of XOR gates for binary to Gray conversion and vice versa
Statement II: Hence forth, the same XOR gates can be used with a gating network and control circuit
a. Both are false
b. Both are true
c. Only I is true
d. Can't be said but II is not dependent on I

13. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0) after the 333rd clock pulse is



a. 00
b. 01
c. 10
d. 11

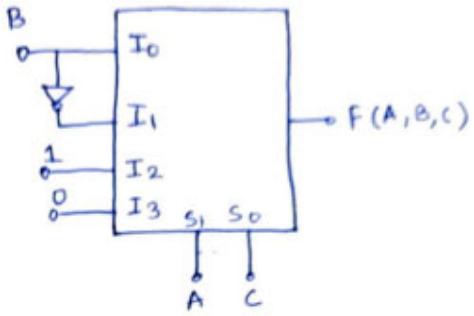
14. To realize the given truth table from the circuit shown in the figure, the input to J in terms of A and B would be have to be



A	B	Q_{n+1}
0	0	$\bar{Q}_n$
0	1	1
1	0	Q_n
1	1	0

a. $\overline{AB}$
b. $\bar{A}$
c. B
d. AB

15. The correct Boolean function implemented by the circuit shown above is –



a. F = Σ(1, 2, 4, 6)
b. F = Σ(1, 3, 4, 7)
c. F = Σ(0, 1, 2, 5)
d. F = Σ(1, 2, 5, 6)

16. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles

a. an AND gate
b. an OR gate
c. an XOR gate
d. a NAND gate

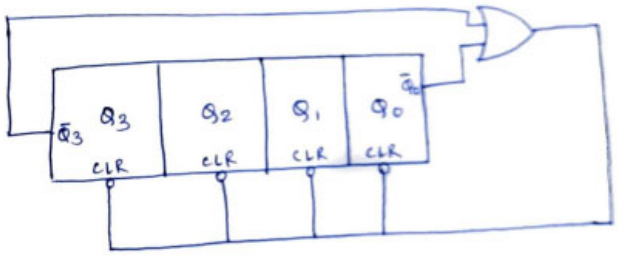
17. If a Mod 14 and Mod 20 counter are cascaded, what will be the new Mod number?

a. 34
b. 280
c. 6
d. Will not be a counter any more

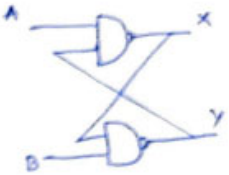
18. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

a. 4
b. 6
c. 8
d. 10

19. The modulus of following asynchronous clear counter is _____.



20. In the figure, A = 1 & B = 1: I/P B is now replaced by a sequence 010101010…., then the outputs X & Y will be



a. Fixed at 0 & 1 respectively
b. X = 101010…., Y = 010101….
c. X = 101010…., Y = 101010….
d. Fixed at 1 & 0 respectively