| | Credit Based Gr | OF INFORMAT | | | |
|------------|--|---|-----------------|---------------------|---------------------------------------|
| INEERS | | CBGS-2012 | | sy or manipar | Estd. 200 |
| TCET/ | FRM/IP-02/10 | Semester (Practical / Tutorials | |) | Revision |
| Semest | ter: III | Course: IT | | Batches: S.E | |
| Subject | : Digital design Lab | Class: SE – I | т | Batch size: 2 | 0 Students |
| Laborat | tory faculty in charge: Mi | r. Zahir Aalam and Ms. | Swati Abhang | | int /Attendant: b Attendant |
| Note: E | xperiment planned as | per University Curric | ulum | | |
| Basic | Experiments: | | | | |
| Sr. No. | Experiments / Tute | LES orials / Assignment se of Technology) | Planned Date | Completio n Date | Remarks |
| 1 | Verify the truth table o and universal gates) | f logic gates (basic | | | |
| 2 | Realization of Boolear | algebra using gates | | | |
| 3 | Verify the operation of comparator | 4- bit magnitude | | | |
| Desig | n/ Development Experi | iments: | | | |
| 4 | Design of Full Adder a | and Full Subtractor | | | |
| 5 | Implementation of Mul Multiplexer using Gate | | | | |
| 6 | Implementation of End using Gates | coder and Decoder | | | |
| | | | | | |
| Issued | d By: MR | ļ | Approved By: P | rincipal | |

| | | TCET | | | L'ANDA | |
|-----------------------|---|---|---|---|---|--|
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| NEERS | | CBGS-2012 | | | Estd. 2001 | |
| 7 | To verify and observe the opera and JK flip-flops | tion of SR | | | | |
| 8 | To design and verify Left and Right shift registers | | | | | |
| 9 | Implementation of Logic Gates u | ising VHDL | | | | |
| Group | D Learning Activity: | | - | | | |
| 10 | Case Study on: Case study on Evaluating and ol Boolean expression using PALs | | | | | |
| 11 | Project: 1. To design automated system machine | for washing | | | | |
| | 2. To design control system for li inor Projects Objective: To get h dent choice in the following areas. | ands on exp | | | | |
| stuc The a | 2. To design control system for linor Projects Objective: To get he dent choice in the following areas. Freas are: 1. Research 2. Cor | ands on exp (30 Hrs / Se re 3. M | mester / Stu ultidisciplina Group Size/ | dent). (Total ⁴ ary 4. App Project | l20 Hrs) | |
| stuc | 2. To design control system for lining Projects Objective: To get he dent choice in the following areas. | ands on exp (30 Hrs / Se | mester / Stu ultidisciplin Group | dent). (Total ⁻ ary 4. App | 120 Hrs) | |
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| stud The a | 2. To design control system for liner Projects Objective: To get here the choice in the following areas. Freas are: 1. Research 2. Cor Project Title/Group Size | iands on exp (30 Hrs / Se re 3. M Class | Group Size/ Project Hours | dent). (Total ⁴ ary 4. App Project Type | l20 Hrs) | |
| stuc The a S.No | 2. To design control system for liner Projects Objective: To get head the choice in the following areas. Freas are: 1. Research 2. Correct Project Title/Group Size Simple Logic Gate Processor | ands on exp (30 Hrs / Se re 3. M Class SE | Group Size/ Project Hours 4-5 | dent). (Total ² ary 4. App Project Type Mini | I20 Hrs) Dication Reference <u>http://circuitea com/logic-gate http://circuitea</u> | |
| stuc The a S.No | 2. To design control system for liner Projects Objective: To get head the choice in the following areas. Freas are: 1. Research 2. Correct Project Title/Group Size Simple Logic Gate Processor | ands on exp (30 Hrs / Se re 3. M Class SE | Group Size/ Project Hours 4-5 | dent). (Total ² ary 4. App Project Type Mini | I20 Hrs) Dication Reference <u>http://circuitea com/logic-gate http://circuitea</u> | |
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| NEERS | LITE | edit Based Grat | | errevise BGS-201 | | | | bai | 00 | Estd. 2001 |
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