TCET/FRM/IP-02/10 Revision: B

Semester Plan
(Practical / Tutorials / Assignment)

Semester: **III** Course: **IT** Batches: **S.E**

Subject: **Logic design Lab** Class: **SE – IT** Batch size: **20** Students

Laboratory faculty in charge: Mr. Zahir Aalam Lab. Assistant /Attendant: Mr. Vaibhav Chavan

Note: **Experiment planned as per University Curriculum**

Basic Experiments:

Sr. No.	TITLES Experiments / Tutorials / Assignment (Planning with use of Technology)	Planned Date A1	Planned Date A3	Completion Date A1	Completion Date A3	Remarks
1	Verify the truth table of logic gates (basic and universal gates)	27/07/17	24/07/17			
2	Realization of Boolean algebra using gates	03/08/17	31/07/17			
3	Verify the operation of 4- bit magnitude comparator	10/08/17	07/08/17			
Design/ Development Experiments:						
4	Design of Full Adder and Full Subtractor	24/08/17	14/08/17			
5	Implementation of Multiplexer and De-Multiplexer using Gates	31/08/17	04/09/17			
6	Implementation of Encoder and Decoder using Gates	07/09/17	11/09/17			
7	To verify and observe the operation of SR and JK flip-flops	14/09/17	18/09/17			

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8	To design and verify Left and Right shift registers	21/09/17	25/09/17			
9	Implementation of Logic Gates using VHDL	05/10/17	07/10/17			
Group Learning Activity:						
10	**Case Study on:** Case study on Evaluating and observing Boolean expression using PALs and PLAs	12/10/17	16/10/17			
11	**Project:** 1. To design automated system for washing machine 2. To design control system for lift	17/10/17	17/10/17			

Bridge courses Objective: Bridging of gaps with respect to prerequisites and industry skills or to carryout research in that particular field**. (24 Hrs / Semester / student)**

S.No	Bridge courses/Technology	Duration (Week/hrs)	Modes of Learning	Recommended Sources
1.	**Prerequisite course:** Logic Building using C/C++ or Java	2 Weeks / 3 Hrs	Self Learning/ Revision	http://www.sunilb.com/programming/5-tips-on-improving-programming-logic
2	**Advanced course:** Advanced Digital Logic Design	12 Weeks / 2 Hrs	Self-Learning/ Revision	http://www.ece.rice.edu/~kmram/elec326/

1. **Mini /Minor Projects Objective:** To get hands on experience to execute projects with respect to student choice in the following areas. **(30 Hrs / Semester / Student). (Total 120 Hrs)**

The areas are:

1. Research **2. Core** **3. Multidisciplinary** **4. Application**

Major project: As per University Scheme

S.No	Project Title/Group Size	Class	Type / Project Hours	Modes of Learning	Reference
1	Simple Logic Gate Processor	SE	Research/ Application	Online and Laboratory	http://circuiteasy.com/logic-gates/

2	Learn to Make NAND Gate			SE	Research/ Application	Online and Laboratory	http://circuiteasy.com/nand-gate

	Planned	Completed		Planned	Completed		Planned	Completed
No. of Prac	**Basic Exp:** 03 **Design Base Exp**: 06 **Group Learning:** 02 **Bridge Course:** 02 **Minor Project:** 02		No. of Assignments	03		No. of Tutorial	NA	

DOSLNE:	DOSLE (engaged in some other dates):

Group activities are required to be added with the practical related to course to enhance the learning activity of the student in the course. Group activity includes: Group presentation, new experiment design, mini projects etc.

Note:

1. The practical plan date and completion date shall be in compliance. For any non-compliance reason(s) required to be stated in remark column.
2. Learning objective and outcome shall be clearly stated with each of experiments/ tutorials/ assignments and are required to be mapped at the end of the semester.
3. Entry for DOSLE (engaged on some other date) shall be done with proper mapping to DOSLNE.

(Mr. Zahir Aalam)

Name & Signature of Faculty	Signature of HOD	Signature of Principal / Dean Academic
Date: 20/07/2017	Date:	Date:

Issued By: MR	Approved By: Principal