TCET DEPARTMENT OF INFORMATION TECHNOLOGY (IT)



Credit Based Grading Scheme(Revised - 2012) - University of Mumbai CBGS-2012(R)



TCET/FRM/IP-02/10

Semester Plan
(Practical / Tutorials / Assignment)

Semester: III	Course: IT	Batches: S.E
Subject: Logic design Lab	Class: SE – IT	Batch size: 20 Students

Laboratory faculty in charge: Mr. Zahir Aalam Lab. Assistant /Attendant: Mr. Vaibhav Chavan

Note: Experiment planned as per University Curriculum

Basic Experiments:

Sr. No.	TITLES Experiments / Tutorials / Assignment (Planning with use of Technology)	Planned Date A1 A3		d Compl Dat 43 A1		Remarks
1	Verify the truth table of logic gates (basic and universal gates)	27/07/17	24/07/17			
2	Realization of Boolean algebra using gates	03/08/17	31/07/17			
3	Verify the operation of 4- bit magnitude comparator	10/08/17	07/08/17			

Design/ Development Experiments:

4	Design of Full Adder and Full Subtractor	24/08/17	14/08/17		
5	Implementation of Multiplexer and De- Multiplexer using Gates	31/08/17	04/09/17		
6	6 Implementation of Encoder and Decoder using Gates		11/09/17		
7	7 To verify and observe the operation of SR and JK flip-flops		18/09/17		
Issued By: MR		Approve	d By: Pi	rincipal	

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8	To design and verify Left and Right registers	t shift	21/09/17	25/09/17			Estd. 2001				
9	Implementation of Logic Gates usir	ng VHDL	05/10/17	07/10/17							
Group	Group Learning Activity:										
10	Case Study on: Case study on Evaluating and obse Boolean expression using PALs an	erving Id PLAs	12/10/17	16/10/17							
11	 Project: 1. To design automated system for machine 2. To design control system for lift 	washin	17/10/17	17/10/17							
Bridge carryou	Bridge courses Objective: Bridging of gaps with respect to prerequisites and industry skills or to carryout research in that particular field. (24 Hrs / Semester / student)										
S.No	S.No Bridge courses/Technology Duration (Week/hrs) Modes of Learning Sources										
1.	Prerequisite course: Logic Building using C/C++ or Java	à	2 We 3 Hrs	2 Weeks / Self Learning/ Revision			http://www.sunilb. com/programmin g/5-tips-on- improving- programming- logic				
2	Advanced course: Advanced Digital Logic Design		12 W 2 Hrs	2 Weeks / Hrs Self- Learning/ Revision			http://www.ece.ric e.edu/~kmram/el ec326/				
1. Mini /Minor Projects Objective: To get hands on experience to execute projects with respect to student choice in the following areas. (30 Hrs / Semester / Student). (Total 120 Hrs) The areas are: 1. Research 2. Core 3. Multidisciplinary 4. Application Major project: As per University Scheme											
S.No	Project Title/Group Size	Class	Type Proje Hour	Type / Project Hours		s of ing	Reference				
1	Simple Logic Gate Processor	SE	Rese Appli	Research/ Application		and atory	http://circuiteasy. com/logic-gates/				
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Service and the second			C	BG2-	2012	(H)					Estd. 2001
2	Learn to Make NAND Gate			SE Research/ Application			Online ar Laborato	nd ry	http://circuiteasy. com/nand-gate		
	Planned	Completed		Planned (Comple	eted		Planned		Completed
No. of Prac	Basic Exp: 03 Design Base Exp: 06 Group Learnin g: 02 Bridge Course: 02 Minor Project: 02		No. of Assign ments	03				No. of Tutorial	NA		
DOSL	NE:				DOSL	E (enga	ged in	some oth	er d	ates):	
 The practical plan date and completion date shall be in compliance. For any non-compliance reason(s) required to be stated in remark column. Learning objective and outcome shall be clearly stated with each of experiments/ tutorials/ assignments and are required to be mapped at the end of the semester. Entry for DOSLE (engaged on some other date) shall be done with proper mapping to DOSLNE. (Mr. Zahir Aalam) Name & Signature of Eaculty 											
D /	The & Signature of Faculty Signature of HOD Signature								noip		
Date.	20/07/201	1									
Issued	By: MR				A	pproved	By: Pi	rincipal			