# TCET

# DEPARTMENT OF INFORMATION TECHNOLOGY (IT)

Credit Based Grading Scheme(Revised - 2012) - University of Mumbai

**CBGS-2012(R)**

Estd. 2001

**Semester Plan**

**TCET/FRM/IP-02/09** **(Theory)** **Revision: A**

**Semester: III** **Course: IT**

**Subject: ITC- 302: Logic Design** **Class: SE IT -B**

| S.No. | Prerequisite/ Bridge course: | Duration (Week /Hrs) | Modes of Learning | Recommended Sources |
|---|---|---|---|---|
| 1 | Semiconductor theory, Diodes, Integrated Circuits | 6 hours | Self Learning/ Revision | **Textbooks:**1. Robert L. Boylestad, Louis Nashelsky, "Electronic devices and circuit Theory", PHI |

## Class Room Teaching

| Sr. No | Module No. | Lesson No | Topics Planned (Technology to be used) | Teaching Aids Required | Planned /Completion Date | Resource Book Reference | Remarks |
|---|---|---|---|---|---|---|---|
| 1 | Module 1 | L1.1 | SOP -Biasing of BJT: DC operating point, | Power point presentation, Chalk & Board | 10/07/17 | 1.10.1 | |
| 2 | Module 1 | L1.2 | SOP -BJT characteristics & parameters | Power point presentation, Chalk & Board | 11/07/17 | 1.10.2 , 1.10.3 | |
| 3 | Module 1 | L1.3 | All biasing circuits, | Power point presentation, Chalk & Board | 12/07/17 | 1.10.4 | |
| 4 | Module 1 | L1.4 | analysis of above circuits and their design, | Power point presentation, Chalk & Board | 13/7/2017 | 1.10.5 | |
| 5 | Module 1 | L1.5 | variation of operation point and its stability. | Power point presentation, Chalk & Board | 14/07/2017 | 1.10.6 | |
| 6 | Module 1 | L1.6 | Differential Amplifier, | Power point presentation, Chalk & Board | 14/07/2017 | 1.10.7 | |
| 7 | Module 1 | L2.1 | constant current source, | Power point presentation, Chalk | 17/07/17 | 1.10.8 | |

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| 8 | Module 1 | L2.2 | current mirror. | Power point presentation, Chalk & Board | 18/07/17 | 1.10.9 | |
| 9 | Module 2 | L23 | Introduction to Number systems, | Chalk & Board, | 18/07/17 | 2 | |
| 10 | Module 2 | L2.4 | Binary Number systems, | Chalk & Board, | 19/7/2017 | 2.8.1 2.8.2 | |
| 11 | Module 2 | L2.5 | Signed Binary Numbers, Binary, Octal, | Chalk & Board, | 20/7/2017 | 2.8.3 | |
| 12 | Module 2 | L 2.6 | Decimal and Hexadecimal number Systems and their conversion | Chalk & Board, | 21/07/2017 | 2.8.4 | |
| 13 | Module 2 | L 3.1 | Binary arithmetic using compliments, | Power point presentation, Chalk & Board | 24/07/2017 | 2.8.5 | |
| 14 | Module 2 | L 3.2 | Gray Code, BCD Code | Chalk & Board, | 25/07/2017 | 2.8.6 | |
| 15 | Module 2 | L 3.3 | Excess-3 code, ASCII Code | Chalk & Board, | 26/07/2017 | 2.8.7 | |
| 16 | Module 2 | L 3.4 | inter-conversion of codes | Chalk & Board, | 27/07/2017 | 2.8.8 | |
| 17 | Module 3 | L 4.1 | Introduction, NAND and NOR operations, Exclusive –OR and Exclusive –NOR operations, | Chalk & Board, | 31/07/2017 | 3.8.1 | |
| 18 | Module 3 | L4.2 | Boolean Algebra Theorems and Properties | Power point presentation, Chalk & Board | 01/08/2017 | 3.8.2 | |
| 19 | Module 3 | L4.3 | Standard SOP and POS form, | Chalk & Board, | 02/08/2017 | 3.8.3 | |
| 20 | Module 3 | L4.4 | Reduction of Boolean functions using Algebraic method, K -map method (2,3,4 Variable) | Chalk & Board, | 3/8/2017 | 3.8.4 3.8.5 | |
| 21 | Module 3 | L5.1 | Reduction of Boolean functions using Algebraic method, K -map method (2,3,4 Variable) | Chalk & Board, | 7/8/2017 | 3.8.4 3.8.5 | |
| 22 | Module 3 | L5.2 | Variable entered Maps, | Chalk & Board, | 8/8/2017 | 3.8.6 | |

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| 23 | Module 3 | L5.3 | Quine Mc Cluskey, | Power point presentation, Chalk & Board | 09/08/2017 | 3.8.7 | |
| 24 | Module 3 | L5.4 | Mixed Logic Combinational Circuits and multiple output function | Chalk & Board, | 10/08/2017 | 3.8.8 | |
| 25 | Module 3 | L6.1 | Basic Digital Circuits: NOT, AND, OR, NAND, NOR, EX-OR, EX-NOR Gates. | Chalk & Board, | 14/08/2017 | 3.8.9 3.8.10 | |
| 26 | Module 3 | L6.2 | Basic Digital Circuits: NOT, AND, OR, NAND, NOR, EX-OR, EX-NOR Gates. | Chalk & Board, | 16/08/2017 | 3.8.9 3.8.10 | |
| 27 | Module 4 | L7.1 | Introduction,Half and Full Adder, | Chalk & Board, | 24/08/2017 | 4.7.1 4.7.2 | |
| 28 | Module 4 | L8.1 | Half and Full Subtractor | Chalk & Board | 30/08/2017 | 4.7.3 | |
| 29 | Module 4 | L8.2 | Four Bit Binary Adder | Chalk & Board, | 31/08/2017 | 4.7.4 | |
| 30 | Module 4 | L9.1 | One digit BCD Adder | Chalk & Board, | 04/09/2017 | 4.7.5 | |
| 31 | Module 4 | L9.2 | code conversion | Chalk & Board, | 5/9/2017 | 4.7.6 | |
| 32 | Module 4 | L9.3 | Encoder and Decoder | Chalk & Board, | 6/9/2017 | 4.7.7 | |
| 33 | Module 4 | L9.4 | Multiplexers and De-multiplexers | Chalk & Board, | 7/9/2017 | 4.7.8 | |
| 35 | Module 4 | L10.1 | Binary comparator (2,3 variable)4-bit Magnitude Comparator IC 7485 and ALU IC74181 | Chalk & Board, | 11/09/2017 | 4.7.9 | |
| 36 | Module 5 | L10.2 | Flip Flops : SR, JK, D, T | Chalk & Board, | 12/09/2017 | 5.7.1 | |
| 37 | Module 5 | L10.3 | master slave flip flop, Truth Table, | Chalk & Board, | 13/09/2014 | 5.7.2 5.7.3 | |
| 38 | Module 5 | L10.4 | excitation table and conversion | Chalk & Board, | 14/09/2017 | 5.7.4 | |

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| 39 | Module 5 | L11.1 | Register: Shift register, SISO, SIPO, PISO, PIPO, | Chalk & Board, | 18/09/2017 | 5.7.5 5.7.6 | |
| 40 | Module 5 | L11.2 | Register: Shift register, SISO, SIPO, PISO, PIPO, | Power point presentation, Chalk & Board | 19/09/2017 | 5.7.5 5.7.6 | |
| 41 | Module 5 | L11.3 | Bi-directional and universal shift register. | Chalk & Board, | 20/09/2017 | 5.7.7 | |
| 42 | Module 5 | L11.4 | Counters: Design of synchronous and asynchronous ,Modulo Counter, | Chalk & Board, | 21/09/2017 | 5.7.8 5.7.9 | |
| 43 | Module 5 | L12.1 | Up Down counter IC 74193 | Chalk & Board, | 25/09/2017 | 5.7.10 | |
| 44 | Module 5 | L12.2 | Ring and Johnson Counter | Chalk & Board, | 26/09/2017 | 5.7.11 | |
| 45 | Module 6 | L13.1 | Introduction to VHDL, | Chalk & Board, | 3/10/2017 | 6.6.1 | |
| 46 | Module 6 | L13.2 | Library, Entity | Power point presentation, Chalk & Board | 04/10/2017 | 6.6.2 | |
| 47 | Module 6 | L13.3 | Architecture Modeling styles | Power point presentation, Chalk & Board | 05/10/2017 | 6.6.3 | |
| 48 | Module 6 | L14.1 | Concurrent and Sequential statements, | Power point presentation, Chalk & Board | 12/10/2017 | 6.6.4 | |
| 49 | Module 6 | L14.2 | data objects and data types, attributes, | Chalk & Board, | 13/10/2017 | 6.6.5 | |
| 50 | Module 6 | L15.1 | design examples for combinational circuits | Chalk & Board, | 16/10/2017 | 6.6.6 | |
| 51 | | | Revison / Practice Session for DL Design | Chalk & Board | 16/10/2017 | | |
| 52 | | | University Paper Discussion Practice session for DL Design | Chalk & Board | 16/10/2017 | | |
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| Remark:<br>Course: | | Syllabus Coverage: | | Practice Session: 2 | | **Content Beyond Syllabus:**Classification of Sequential circuits by using Mealy and | |
| No. of (lectures planned)/(lecture taken): 52 | | | | | | | |

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| **Advanced course:**Advanced Digital Logic Design | 20 Hours | Online notes and handouts for | **Web sources:**http://www.ece.rice.edu/~kmram/elec326/ |

Text Books:

**Digital Reference:**

*3.1 www.nptel.ac.in*

3.2www.tutorialpoint.com

Sd/-

Swati Abhang Sd/- Sd/-

Name & Signature of Faculty | Signature of HOD | Signature of Principal /Dean (Academics)

Date: | Date: | Date:

**Note:**

1. Plan date and completion date should be in compliance

2. Courses are required to be taught with emphasis on resource book, course file, text books, reference books, digital references etc.

3. Planning is to be done for 15 weeks where 1st week will be AOP, 2nd-13th for effective teaching and 14th-15th week for effective university examination oriented teaching, mock practice session and semester consolidation.

4. According to university syllabus where lecture of 4 hrs/per week is mentioned minimum 55 hrs and in case of 3 lectures per week minimum 45 lectures are to be engaged are required to be engaged during the semester and therefore accordingly semester planning for delivery of theory lectures shall be planned.

5. In order to improve score in NBA, faculty members are also required to focus course teaching beyond university prescribed syllabus and measuring the outcomes w.r.t learning course and programme objectives.

6. Text books and reference books are available in syllabus. Here only additional references w.r.t. non –digital/ digital sources can be written (if applicable)

7. Technology to be used in class room during lecture shall be written below the topic planned within the bracket.