TCET

DEPARTMENT OF INFORMATION TECHNOLOGY (IT)

Credit Based Grading Scheme(Revised - 2012) - University of Mumbai

CBGS-2012(R)

TCET/FRM/IP-02/09

Semester Plan (Theory)

Revision: A

Semester: III

Course: IT

Subject: ITC-302 : Logic Design

Class: SE IT -A

S.No.	Prerequisite/ Bridge course:	Duration (Week /Hrs)	Modes of Learning	Recommended Sources
1	Semiconductor theory, Diodes, Integrated Circuits	6 hours	Self Learning/ Revision	Robert L. Boylestad, Louis Nashelsky, "Electronic devices and circuit Theory", PHI

Class Room Teaching

Sr. No	Module No.	Lesson No	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion	Resource Book	Remarks
1	2	L1.1	**SOP:** Introduction to Number systems	Chalk and Board	10/7/2017 10/7/2017	2	
2	2	L2.1	Binary Number systems	Chalk and Board	17/7/2017 17/7/2017	2.8.1 2.8.2	
3	2	L2.2	Signed Binary Numbers, Binary, Octal	Chalk and Board	18/7/2017 18/7/2017	2.8.3	
4	2	L2.3	Decimal and Hexadecimal number Systems and their conversion	Chalk and Board	19/7/2017 19/7/2017	2.8.4	
5	2	L2.4	Binary arithmetic using compliments	Chalk and Board	19/7/2017 19/7/2017	2.8.5	
6	2	L2.5	Gray Code, BCD Code	Chalk and Board	20/7/2017 20/7/2017	2.8.6	
7	2	L2.6	Excess-3 code, ASCII Code	Chalk and Board	20/7/2017 20/7/2017	2.8.7	
8	2	L2.7	Inter-conversion of codes	Chalk and Board	21/7/2017	2.8.8	
9	3	L2.8	Introduction, NAND and NOR operations, Exclusive –OR and Exclusive –NOR operations	Chalk and Board	21/7/2017	3.8.1	
10	3	L3.1	Boolean Algebra Theorems and Properties	Chalk and Board	25/7/2017	3.8.2	
11	3	L3.2	Standard SOP and POS form	Chalk and Board	26/7/2017	3.8.3	
12	3	L3.3	Reduction of Boolean functions using Algebraic method, K -map method (2,3,4 Variable)	Chalk and Board	27/7/2017	3.8.4 3.8.5	
13	3	L3.4	Reduction of Boolean functions using Algebraic method, K -map method (2,3,4 Variable)	Chalk and Board	28/7/2017	3.8.4 3.8.5	
14	3	L4.1	Variable entered Maps	Chalk and Board	1/8/2017	3.8.6	
15	3	L4.2	Quine Mc-Cluskey	Chalk and Board	2/8/2017	3.8.7	
16	3	L4.3	Mixed Logic Combinational Circuits and multiple output function	Chalk and Board	3/8/2017	3.8.8	
17	3	L4.4	Basic Digital Circuits: NOT, AND, OR Gates	Chalk and Board	4/8/2017	3.8.9 3.8.10	
18	3	L5.1	Basic Digital Circuits: NAND, NOR, EX-OR, EX-NOR Gates	Chalk and Board	8/8/2017	3.8.9 3.8.10	

19	1	L5.2	BJT characteristics & parameters	Chalk and Board	9/8/2017	1.10.1	
20	1	L5.3	BJT characteristics & parameters	Chalk and Board	10/8/2017	1.10.2 1.10.3	
21	1	L5.4	All biasing circuits	Chalk and Board	11/8/2017	1.10.4	
22	1	L6.1	Analysis of biasing circuits and their design	Chalk and Board	16/8/2017	1.10.5	
23	1	L6.2	Variation of operation point and its stability	Chalk and Board	18/8/2017	1.10.6	
24	1	L6.3	Differential Amplifier	Chalk and Board	19/8/2017	1.10.7	Extra Lecture
25	1	L6.4	Constant current source circuit	Chalk and Board	19/8/2017	1.10.8	Extra Lecture
26	1	L6.5	Current mirror circuit	Chalk and Board	19/8/2017	1.10.9	Extra Lecture
27	4	L7.1	Introduction, Half and Full Adder	Chalk and Board	24/8/2017	4.7.1 4.7.2	Term Test-1
28	4	L8.1	Half and Full Subtractor	Chalk and Board	30/8/2017	4.7.3	
29	4	L8.2	Four bit Binary Adder	Chalk and Board	31/8/2017	4.7.4	
30	4	L8.3	One digit BCD Adder and Code conversion	Chalk and Board	1/9/2017	4.7.5 4.7.6	
31	4	L9.1	Encoder and Decoder	Chalk and Board	5/9/2017	4.7.7	
32	4	L9.2	Multiplexers and De-multiplexers	Chalk and Board	6/9/2017	4.7.8	
33	4	L9.3	Binary comparator (2,3 variable) 4-bit	Chalk and Board	7/9/2017	4.7.9	
34	4	L9.4	Magnitude Comparator IC 7485 and ALU IC74181	Chalk and Board	8/9/2017	4.7.9	
35	5	L10.1	Flip Flops : SR, JK, D, T	Chalk and Board	12/9/2017	5.7.1	
36	5	L10.2	Master slave flip flop, Truth Table	Chalk and Board	13/9/2017	5.7.2 5.7.3	
37	5	L10.3	Excitation table and conversion	Chalk and Board	14/9/2017	5.7.4	
38	5	L10.4	Register: Shift register, SISO, SIPO	Chalk and Board	15/9/2017	5.7.5	
39	5	L10.5	Register: Shift register, PISO, PIPO	Chalk and Board	16/9/2017	5.7.6	Extra Lecture
40	5	L10.6	Bi-directional and universal shift register	Chalk and Board	16/9/2017	5.7.7	Extra Lecture
41	5	L10.7	Counters: Design of synchronous and asynchronous, Modulo Counter	Chalk and Board	16/9/2017	5.7.8 5.7.9	Extra Lecture
42	5	L11.1	Up/Down counter IC 74193	Chalk and Board	19/9/2017	5.7.10	
43	5	L11.2	Ring and Johnson Counter	Chalk and Board	20/9/2017	5.7.11	
44	6	L11.3	Introduction to VHDL	Chalk and Board	21/9/2017	6.6.1	
45	6	L11.4	Library, Entity	Chalk and Board	22/9/2017	6.6.2	
46	6	L12.1	Architecture Modeling styles	Chalk and Board	26/9/2017	6.6.3	Zephyr 2017
47	6	L13.1	Concurrent and Sequential statements	Chalk and Board	3/10/2017	6.6.4	
48	6	L13.2	Data objects and data types, attributes	Chalk and Board	4/10/2017	6.6.5	
49	6	L13.3	Design examples for combinational circuits	Chalk and Board	5/10/2017	6.6.6	

50	6	L13.4	Design examples for combinational circuits	Chalk and Board	6/10/2017	6.6.6	
51		L13.5	Revison / Practice Session for DL Design	Chalk and Board	7/10/2017		Extra Lecture
52		L13.6	Revison / Practice Session for DL Design	Chalk and Board	7/10/2017		Extra Lecture
53		L14.1	University Paper Discussion	Chalk and Board	12/10/2017		
54		L14.2	University Paper Discussion	Chalk and Board	13/10/2017		Term Test-2
Remark:							
Course:		Syllabus Coverage:		Practice Session: 2		**Content Beyond Syllabus:**Classification of Sequential circuits by using Mealy and Moore state machine	
No. of (lectures planned)/(lecture taken): 54							

Advanced course: Advanced Digital Logic Design	20 Hours	Online notes and handouts for the topics	**Web sources:**http://www.ece.rice.edu/~kmram/elec326/

Text Books:

1. Robert L. Boylestad, Louis Nashelsky, “Electronic devices and circuit Theory”, PHI
2. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.
3. M. Morris Mano, “Digital Logic and computer Design”, PHI
4. J. Bhasker.“ VHDL Primer”, Pearson Education.
5. Balbaniam,Carison,”Digital Logic Design Principles”, Wiley Publication

References:

1. Martin s. Roden, Gordon L. Carpenter, William R. Wieserman “Electronic Design-From Concept to Reality”, Shroff Publishers and Distributors. 2. A. Anand Kumar, “Fundamentals of Digital Circuits ”, Prentice Hall India 3. Subrata Ghosal, ”Digital Electronics”, Cengage Learning.
4. Anil K. Maini, “Digital Electronics Principles and Integrated Circuits”, Wiley India
5. Donald p Leach, Albert Paul Malvino, “Digital principles and Applications”, Tata McGraw Hill

Digital Reference:

1. www.nptel.ac.in
2. www.tutorialpoint.com

Zahir Aalam

Name & Signature of Faculty Signature of HOD Signature of Principal /Dean (Academics)

Date: 20/07/2017 Date: Date:

Note:

1. Plan date and completion date should be in compliance
2. Courses are required to be taught with emphasis on resource book, course file, text books, reference books, digital references etc.
3. Planning is to be done for 15 weeks where 1st week will be AOP, 2nd-13th for effective teaching and 14th-15th week for effective university examination oriented teaching, mock practice session and semester consolidation.
4. According to university syllabus where lecture of 4 hrs/per week is mentioned minimum 55 hrs and in case of 3 lectures per week minimum 45 lectures are to be engaged are required to be engaged during the semester and therefore accordingly semester planning for delivery of theory lectures shall be planned.
5. In order to improve score in NBA, faculty members are also required to focus course teaching beyond university prescribed syllabus and measuring the outcomes w.r.t learning course and programme objectives.
6. Text books and reference books are available in syllabus. Here only additional references w.r.t. non –digital/ digital sources can be written (if applicable)
7. Technology to be used in class room during lecture shall be written below the topic planned within the bracket.